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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,200	09/25/2003	Christian Dupuy	ATM-240	6943

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SCHNECK & SCHNECK
P.O. BOX 2-E
SAN JOSE, CA 95109-0005

EXAMINER	
NGUYEN, HAI L	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 09/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/671,200	DUPUY ET AL.	
	Examiner	Art Unit	
	Hai L. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-10* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/30/03, 1/02/04, 4/05/04, and 04/12/04*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Fig. 3 is objected to because the common mode voltages are labeled "ISENSE1" and "ISENSE2" instead of "Vsense1" and "Vsense2" as disclosed in the specification (pages 4-5); and "Resistors 446 and 444" should be changed to --Resistors **442** and 444--.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: the current source I1 in Fig. 3.

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: The reference current **I0**. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. The disclosure is objected to because of the following informalities: the spacing of the words of the specification is such as to make reading/OCRing difficult, a new application papers

with cleared spaced between words is required; "second transistor 430" (p.4 lines 32-33) should be changed to --second transistor 424—as shown in Fig. 3.

Claim Objections

5. Claim 5 is objected to because of the following informalities:

line 4, "a anode terminal" should be changed to --**an** anode terminal--;

line 8, "the current means" should be changed to --the current **source** means--;

lines 9-10, "a voltage source" should be changed to --**the low** voltage source--; and

last line, "current source" should be changed to --current source means--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 2-3 and 6-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 is indefinite because of the limitation "a drain of the third NMOS transistor being coupled to a third NMOS transistor" is unclear. It is not clear which preferred embodiment is referred to by the claimed limitation.

Claim 3 is indefinite because the recited limitations "a fourth resistor" and "a fifth resistor", on lines 8-10, lacks antecedent basis since there is no first or second or third resistor.

8. Claim 6 recites the limitation "the current mirror means" in line 8. There is insufficient antecedent basis for this limitation in the claim.

9. Claims 7-10 are rejected due to their dependencies on claim 6.

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 1 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Whittaker et al. (US 6,483,345).

With respect to claim 1, Whittaker et al. discloses in Fig. 2 a circuit coupled to an external sensing resistor (R9, R10), a low voltage source (LOW VOLTAGE POWER SUPPLY) and a high voltage source (CHIP POWER SUPPLY), comprising current source means for creating a reference current and mirror currents (currents through Q5, Q6, Q7) based on the high voltage source; and means for current-to-voltage conversion (200) coupled to the current source for rejecting the high voltage signal and converting the current caused by the low voltage signal that flows through the sensing resistor into a voltage proportional to the low voltage source.

With respect to claim 4, the interface further comprises means for electrostatic discharge protection (R1, C1, R2, C2).

Allowable Subject Matter

12. Claim 3 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

13. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

14. Claims 6-10 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

The prior art of record fails to disclose or fairly suggest the means for current-to-voltage conversion (460 in instant Fig.3), as recited in claim 3, comprising a specific structural limitations such as an operational amplifier (440) with the non-inverting input terminal and the inverting input terminal being coupled to the current source (422, 424, 426, 430, 432, 434); the output terminal of the op-amp being coupled to the inverting input terminal through a fourth resistor (442); the non-inverting terminal being coupled to an external reference voltage source (446) through a fifth resistor (444); a first DC couple terminal of the op-amp being coupled to an external voltage source (**VDD**) for setting the upper voltage limit for the op-amp, a second DC couple terminal being coupled to the electrical ground for setting a lower voltage limit for the op-amp; and being configured in a high-to-low voltage interface integrated circuit coupled to the external sensing resistor (414), low voltage source and high voltage sources (**VDD**, **VHV**), comprising current source means (420).

The prior art of record fails to disclose or fairly suggest the means for ESD protection, as recited in claim 5, comprising a specific structural limitations such as a first and second pn junction devices (482-492 in instant Fig.3) coupled in series to one another and to the current source, an anode terminal of the first pn junction device (484, 488, 492) being coupled to the electrical ground and a cathode terminal of the first pn junction device being coupled to the anode terminal of the second pn junction device and to the current source means (422, 424, 426, 430, 432, 434), the cathode terminal of second pn junction device being coupled to the low voltage source (**VDD**) for prevent ESD discharge therefrom into the current source means (420); and being configured in a high-to-low voltage interface integrated circuit coupled to the external sensing resistor (414), low voltage source and high voltage sources (**VDD**, **VHV**).

The prior art of record fails to disclose or fairly suggest an external RC low pass filters (502-510 in instant Fig.3), as recited in claim 6, being coupled to the sensing resistor (414), a low voltage signal (**VDD**), a high voltage signal (**VHV**), so as to filter out high frequency signals therefrom, and being configured in a high-to-low voltage interface integrated circuit (420, 460).

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. For example, Carvajal (US 5,276,358) is cited as of interest because it discloses a circuitry and method for controlling voltage in an electronic circuit.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hai L. Nguyen whose telephone number is 571-272-1747 and

Right Fax number is 571-273-1747. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The official fax phone number for the organization where this application or proceeding is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-1562.

HLN
September 22, 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800